R. J. Widlar
National Semiconductor

LINEAR BRIEF 6

FAST VOLTAGE COMPARATORS WITH LOW INPUT CURRENT

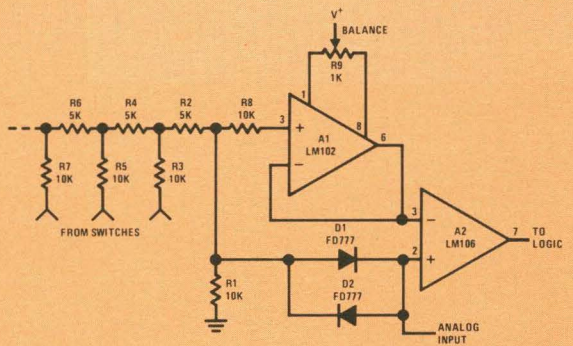
Monolithic voltage comparators are available today which are both fast and accurate. They can detect the height of a pulse with a 5 mV accuracy within 40 ns. However, these devices have relatively high input currents and low input impedances, which reduces their accuracy and speed when operating from high source resistances. This is probably a basic limitation since the input transistors of the integrated circuit must be operated at a relatively high current to get fast operation. Further, the circuit must be gold doped to reduce storage time, and this limits the current gain that can be obtained in the transistors. High gain transistors operating at low collector currents are necessary to get good input characteristics.

One way of overcoming this difficulty is to buffer the input of the comparator. A voltage follower is available which is ideally suited for this job. This device, the LM102*, is both fast and has a low input current. It can reduce the effective input current of the comparator by more than three orders of magnitude without greatly reducing speed.

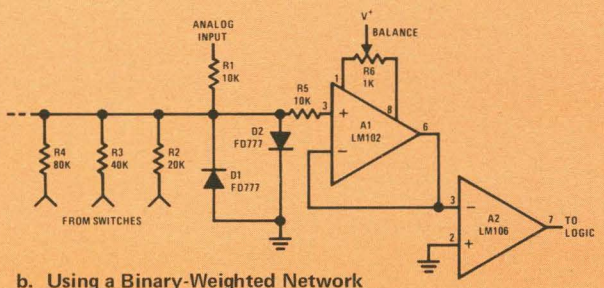
A comparator circuit for an A/D converter which uses this technique is shown in Figure 1a. An LM102 voltage follower buffers the output of a ladder network and drives one input of the comparator. The analog signal is fed to the other input of the comparator. It should come from a low impedance source such as the output of a signal processing amplifier, or another LM102 buffer amplifier.

Clamp diodes, D_1 and D_2, are included to make the circuit faster. These diodes clamp the output of the ladder so that it is never more than 0.7V different from the analog input. This reduces the voltage excursion that the buffer must handle on the most significant bit and keeps it from slewing. If fast, low-capacitance diodes are used, the signal to the comparator will stabilize approximately 200 ns after the most significant bit is switched in. This is about the same as the stabilization time of the ladder network alone, as its speed is limited by stray capacitances. The diodes also limit the voltage swing across the inputs of the comparator, increasing its operating speed and insuring that the device is not damaged by excessive differential input voltage.

The buffer reduces the loading on the ladder from 45 μA to 20 nA, maximum, over a −55°C to 125°C temperature range. Hence, in most applications the input current of the buffer is totally insignificant. This low current will often permit



a. Using a Ladder Network



b. Using a Binary-Weighted Network

FIGURE 1. Comparator Circuits for Fast A/D Converters

the use of larger resistances in the ladder which simplifies design of the switches driving it.

It is possible to balance out the offset of the LM102 with an external 1 kΩ potentiometer, R_9. The adjustment range of this balance control is large enough so that it can be used to null out the offset of both the buffer and the comparator. A 10 kΩ resistor should be installed in series with the input to the LM102, as shown. This is required to make the short circuit protection of the device effective and to insure that it will not oscillate. This resistor should be located close to the integrated circuit.

A similar technique can be used with A/D converters employing a binary-weighted resistor network. This is shown in Figure 1b. The analog input is fed into a scaling resistor, R_1. This resistor is selected so that the input voltage to the LM102 is zero when the output of the D/A network corresponds to the analog input voltage. Hence, if the D/A output is too low, the output of the LM106 will be a logical zero; and the output will change to a logical one as the D/A output exceeds the analog signal.

The analog signal must be obtained from a source impedance which is low by comparison to R_1. This can be either another LM102 buffer or the output of the signal-processing amplifier. Clamp diodes, D_1 and D_2, restrict the signal swing and speed up the circuit. They also limit the input signal seen by the LM106 to protect if from over-

*R. J. Widlar, "A Fast Integrated Voltage Follower," *National Semiconductor Corporation AN-8*, May, 1968.

©1969 NATIONAL SEMICONDUCTOR CORP.

LINEAR BRIEF 6 FAST VOLTAGE COMPARATORS WITH LOW INPUT CURRENT

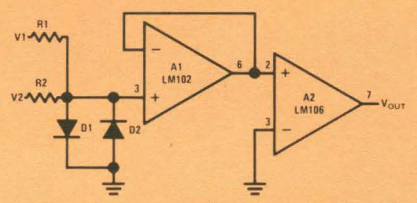
loads. Operating speed can be increased even further by using silicon backward diodes (a degenerate tunnel diode) in place of the diodes shown, as they will clamp the signal swing to about 50 mV. The offset voltage of both the LM102 and the LM106 can be balanced out, if necessary, with R_6.

The binary weighted network can be driven with single pole, single throw switches. This will result in a change in the output resistance of the network when it switches, but circuit performance will not be affected because the input current of the LM102 is negligible. Hence, using the LM102 greatly simplifies switch design.

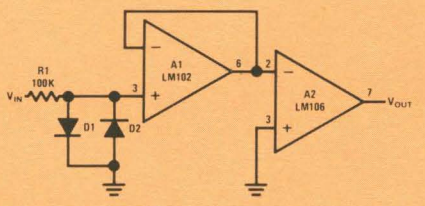
Although it is possible to use a 710 as the voltage comparator in these circuits, the LM106 offers several advantages. First, it can drive a fan out of 10 with standard, integrated DTL or TTL. It also has two strobe terminals available which disable the comparator and give a high output when either of the terminals is held at a logical zero. This adds logic capability to the comparator in that it makes it equivalent to a 710 and a two-input NAND gate. If not needed, the strobe pins can be left unconnected without affecting performance. The voltage gain of the LM106 is about 45,000, which is 30 times higher than that of the 710. The increased gain reduces the error band in making a comparison. The LM106 will also operate from the same supply voltage as the LM102, and other operational amplifiers, for ±12V supplies. However, it can also be operated from ±15V supplies if a 3V zener diode is connected in series with the positive supply lead.

It is necessary to observe a few precautions when working with fast circuits operating from relatively high impedances. A good ground is necessary, and a ground plane is advisable. All the individual points in the circuit which are to be grounded, including bypass capacitors, should be returned separately to the same point on the ground so that voltages will not be developed across common lead inductance. The power supply leads of the integrated circuits should also be bypassed with low inductance 0.01 μF capacitors. These capacitors, preferably disc ceramic, should be installed with short leads and located close to the devices. Lastly, the output of the comparator should be shielded from the circuitry on the input of the buffer, as stray coupling can also cause oscillation.

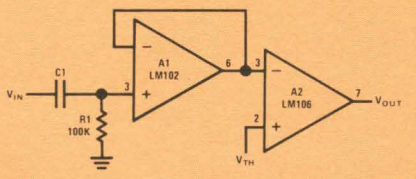
Although the circuits shown so far were designed for use in A/D converters, the same techniques apply to a number of other applications. Figure 2 gives examples of circuits which can put stringent input current requirements on the comparator. The first is a comparator for signals of opposite



a. Comparator for Signals of Opposite Polarity



b. Zero Crossing Detector



c. Comparator for AC Coupled Signals

FIGURE 2. Applications Requiring Low Input Current Comparators

polarity. Resistors (R_1 and R_2) are required to isolate the two signal sources. Frequently, these resistors must be relatively large so that the signal sources are not loaded. Hence, the input current of the comparator must be reduced to prevent inaccuracies. Another example is the zero-crossing detector in Figure 2b. When the input signal can exceed the common mode range of the comparator (±5V for the LM106), clamp diodes must be used. It is then necessary to isolate the comparator from the input with a relatively large resistance to prevent loading. Again, bias currents should be reduced. A third example, in Figure 2c, is a comparator with an ac coupled input. An LM106 will draw an input current which is twice the specified bias current when the signal is above the comparison threshold. Yet, it draws no current when the signal is below the threshold. This asymmetrical current drain will charge any coupling capacitor on the input and produce an error. This problem can be eliminated by using a buffer, as the input current will be both low and constant.

The foregoing has shown how two integrated circuits can be combined to provide state-of-the-art performance in both speed and input current. Equivalent results will probably not be achievable in a single circuit for some time, as the technologies required are not particularly compatible. Further, considering the low cost of monolithic circuits, approaches like this are certainly economical.

National Semiconductor Corporation
2975 San Ysidro Way, Santa Clara, California 95051
(408) 245-4320/TWX (910) 339-9240

5-69 PRINTED IN U.S.A.